Amendment to the Specification:

Please replace paragraph [0016] with the following amended paragraph:

"[0016] Device 400 asserts interrupt signal 410 that is communicated to host monitor 420. **The host monitor 420 may be implemented at least in part as an article comprising a set of instructions on a computer-accessible storage medium to be executed by one or more processors performing the functions of the host monitor 420. The interface which the host monitor 420 provides between the hardware of the host machine and the virtual machines 440, 450, 460 may include a memory controller 495 communicatively coupled to the host machine 420.** Interrupt signal 410 is communicated to host monitor, at least in part, over a shared interface, for example, a bus conforming to certain versions of the PCI standards. When host monitor 420 responds to an interrupt signal assertion, an interrupt status bit corresponding to each of the devices sharing the interrupt signal are checked to determine the source of the interrupt signal. The PCI Local Bus Specification, Revision 2.3 published March 29, 2002 as well as the PCI Express Base Specification, Version 1.0 published July 23, 2002 and Version 1.0a published October 7, 2003 define an interrupt status bit in the PCI Status register of devices conforming to these specifications. For example, the interrupt status bit is defined as bit 3 of the device status register in Section 6.2 PCI Local Bus Specification, Revision 2.3. Subsequent standards may also define the interrupt status bit or provide another interrupt status indication that can be used as described herein."